Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Original): A method comprising:

predicting a first event that allows for lower performance in a processor;

transitioning said processor from a high performance state to a low performance state upon prediction of said first event;

detecting a second event that can utilize greater performance in said processor; and

transitioning said processor from said low performance state to said high performance state upon detection of said second event.

Claim 2 (Original): The method of claim 1 further comprising detecting a cache miss event.

Claim 3 (Original): The method of claim 2 wherein said cache miss event causes said processor to fetch data from external memory.

Claim 4 (Original): The method of claim 3 wherein said detecting a second event comprises monitoring a bus unit for notification of incoming data from a memory fetch.

Claim 5 (Original): The method of claim 3 wherein said cache miss event causes said processor to stall an instruction pipeline.

Claim 6 (Original): The method of claim 1 wherein said predicting comprises monitoring processor signals indicating a cache miss, processor reset, or standby.

Claim 7 (Original): The method of claim 6 wherein said transitioning from a high performance state to a low performance state comprises powering down idle functional units in said processor.

Claim 8 (Original): The method of claim 1 wherein said high performance state consumes a greater amount of power than said low performance state.

Claim 9 (Original): The method of claim 8 wherein said transitioning from a high performance state to a low performance state comprises powering down functional units that are not in use.

Claim 10 (Original): The method of claim 9 wherein said transitioning from said low performance state to said high performance state comprises powering up functional units that have been powered down.

Claim 11 (Original): The method of claim 8 wherein said transitioning from a high performance state to a low performance state further comprises slowing down an internal processor core clock signal from a normal operating frequency to a lower frequency.

Claim 12 (Original): The method of claim 11 wherein said transitioning from said low performance state to said high performance state comprises speeding up said internal processor core clock signal to said normal operating frequency.

Claim 13-19 (Cancelled)

Claim 20 (Currently amended): A system comprising:

a memory coupled to a bus;

a memory controller coupled to said bus;

a processor coupled to said bus, said processor including control logic to ~~determine~~ predict whether a first event has enabled said processor to be in a low performance state, to transition said processor from a high performance state to said low performance state if said first even has occurred; to detect a second event necessitating said processor to be in said high performance state; and to transition said processor from said low performance state to said high performance state if said second event is detected.

Claim 21 (Original): The system of claim 20 wherein said first event is a cache miss, wherein said cache miss causes said processor to fetch data from said memory.

Claim 22 (Original): The system of claim 21 wherein said second event is bus activity due to a memory read wherein said memory is sending data to said processor.

Claim 23 (Original): The system of claim 22 wherein said control logic is monitoring an data fetch unit within said processor for cache misses and wherein said control unit is monitoring a bus unit within said processor for bus activity with said memory.

Claim 24 (Original): The system of claim 20 further comprising a power supply to provide power to said memory, said memory controller, and said processor.

Claim 25 (Original): The system of claim 24 wherein said power supply can sink current during a transition from a high power state to a low power state, and wherein said power supply can provide current during a transition from said low power state to said high power state.

Claim 26 (Currently Amended): An article comprising a machine readable medium having stored thereon a plurality of instructions which, if executed by a machine, cause the machine to perform a method comprising:

~~determining~~ predicting whether a first event has enabled a processor to operate in a low performance state;

transitioning said processor from a high performance state to said low performance state if said first event has occurred;

detecting a second event that can necessitates greater performance in said processor; and

transitioning said processor from said low performance state to said high performance state upon detection of said second event.

Claim 27 (Original): The article of claim 26 wherein said first event is a cache miss, wherein said cache miss causes said processor to fetch data from memory external to said processor.

Claim 28 (Original): The article of claim 27 wherein said second event is bus activity resulting from said memory send data to said processor.

Claim 29 (Original): The article of claim 28 wherein said method further comprises monitoring said processor for cache misses and monitoring a bus for bus activity.

Claim 30 (Original): The article of claim 26 wherein said machine readable medium is a read only memory (ROM).